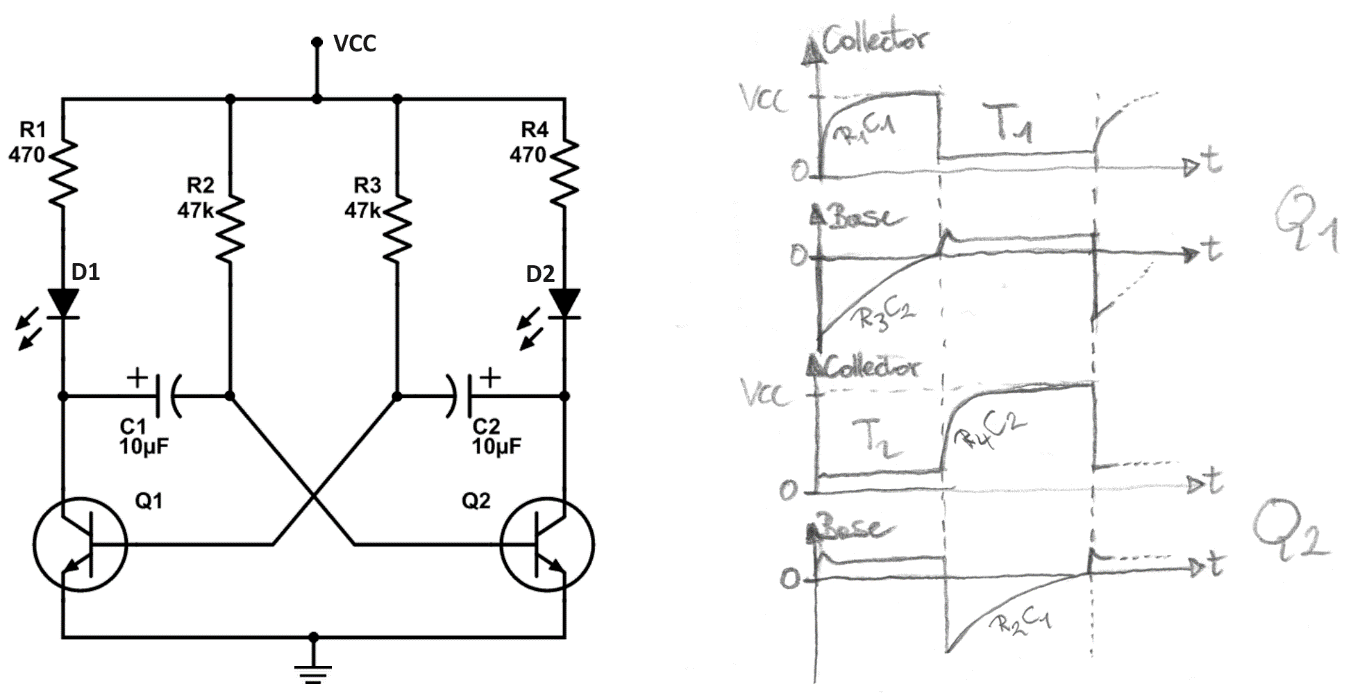
**Analog astable multivibrator**



Note: the D1 and D2 LEDs are optional and VCC <= 5V (for higher voltages see *PWM circuit design* later on).

Initial phase

1. When first powering the circuit both transistors Q1 and Q2 or OFF.
2. There is a race between the two transistors, current flows through R1→C1 (also a bit through R2) into Q2’s BE-junction and through R4→C2 (also a bit through R3) into Q1’s BE-junction. Both capacitors are charging up. Let’s assume Q2 turns ON first.
3. As Q2 turns ON, the collector side of C2 becomes 0V and thus VBE1 is negative, so Q1 is definitively out of the race!

Attention: if the circuit is temporarily held with one base high, for longer than it takes to reverse charge the caps, then the circuit will remain in a stable lock-up state, with both bases at 0.6V, both collectors at 0V, and both capacitors charged backwards to −0.6V. In “Pulse, Digital and Switching Waveforms” book, Millman and Taub tell us at p.441 that this lock-up can also happen spontaneously if the power supply voltage rises slowly from 0V to VCC (note that I could not reproduce that in my laboratory experiments).

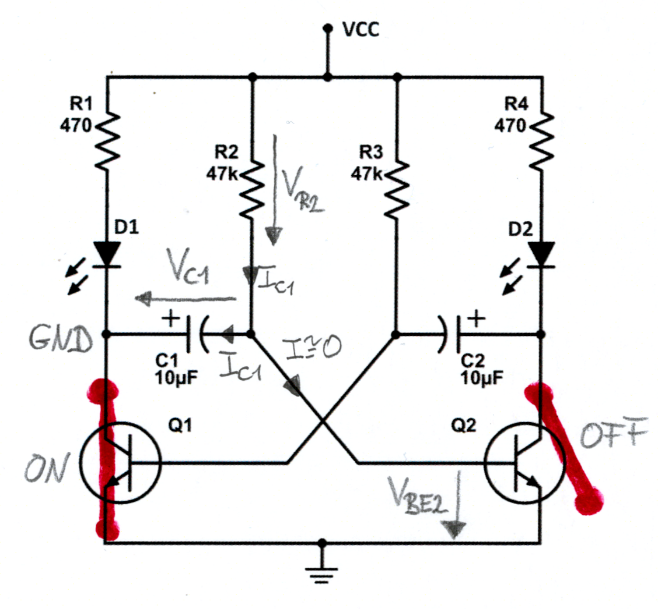
Repetitive phases

1. At first C2 discharges through R3→C2→Q2 and then through the same path it gets charged in reverse to around 0.6V (such a low reverse voltage on an electrolytic capacitor is not a problem). In this phase the optional D2 is ON thanks to the R4→D2→Q2 path.
2. Q1 turns ON, the collector side of C1 becomes 0V and thus VBE2 is negative, Q2 turns OFF. C2 charges quite fast through the small R4 and Q1’s BE-junction, so Q1 enters saturation. After C2 is fully charged there is still enough current flowing into the Q1 base through R3.
3. At first C1 discharges through R2→C1→Q1 and then through the same path it gets charged in reverse to around 0.6V (such a low reverse voltage on an electrolytic capacitor is not a problem). In this phase the optional D1 is ON thanks to the R1→D1→Q1 path.
4. Q2 turns ON, the collector side of C2 becomes 0V and thus VBE1 is negative, Q1 turns OFF. C1 charges quite fast through the small R1 and Q2’s BE-junction, so Q2 enters saturation. After C1 is fully charged there is still enough current flowing into the Q2 base through R2.

Frequency and duty-cycle

It doesn’t matter which state we look at; the calculations give the same results. Let’s take the moment when transistor Q1 just started to conduct: C1 discharges and charges through R2. For the mathematical derivation we use the well-known formulas of the capacitor charging through a resistor. For the initial conditions we have to remember that the capacitor is already charged.

To make it more readable, instead of C1 and R2 we use C and R without subscripts:



Let’s find the time T when Q2 starts to conduct:

As VBE << VCC we can approximate to:

We re-introduce the subscripts and define T1 the time when Q1 is ON and T2 the time when Q2 is ON:

We simplify with C=C1=C2:

When the R1C1 charging is ending, the current diminishes and Q2 remains ON thanks to R2:

When the R4C2 charging is ending, the current diminishes and Q1 remains ON thanks to R3:

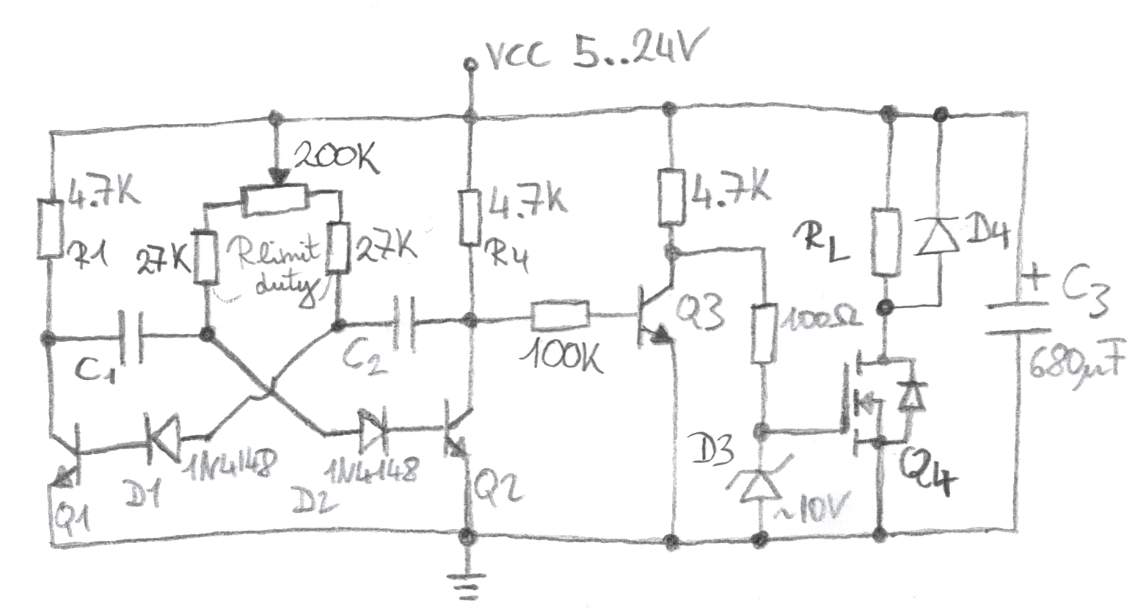
Before T2 ends, the R1C1 charging must reach ~ 98%:

Before T1 ends, the R4C2 charging must reach ~ 98%:

PWM circuit design

By employing a trimpot for R2 and R3, it’s possible to regulate the duty-cycle leaving the frequency constant:

As explained at the beginning, the bases of Q1 or Q2 must never be forced to high, for this reason we need two additional resistors connected with the trimpot.



The trimpot of 200k with the two Rlimit,duty of 27k satisfy the two conditions exposed in previous section:

1. 5.8x4.7k < Rlimit,duty
2. 200k+Rlimit,duty < βx4.7k

The chosen resistor values allow us to regulate the duty-cycle between ~10% and ~90% and work well with C1=C2 from 1µF to 1nF (for example 100nF=~57Hz, 33nF=~172Hz, 10nF=~570Hz).

For a stable and long-lasting circuit please regard these annotations:

* VCC > 5V: D1 and D2 are necessary to avoid the BE-junctions breakdown
* VCC > 12V: D3 zener diode of ~10V is necessary to limit VGS
* D4: necessary for inductive loads like motors or relays, for example 1N4007
* Q1, Q2, Q3: common NPN transistors, for example 2N2222 or BC547
* Q4: n-ch MOSFET with VGS(th) ~2-4V and low RDS(on), for example IRF1404
* C3: choose according to load and audible noise made by power supplies
* R1, R4: are bigger than usual, because otherwise at 24V they would heat-up too much